

13 one of said side walls and a third portion formed over at least a first portion of said top surface of  
14 said floating gate and being separated from said floating gate by said second insulation layer,  
15 said second portion having a surface substantially parallel to and opposing said first side wall;  
16 an erase gate formed over a second one of said side walls and over at least a second  
17 portion of said top surface of said floating gate and being separated from said second one of said  
18 side walls and said portion of said top surface of said floating gate by said second insulation  
19 layer;  
20 a drain region formed in a portion of said substrate proximate said control gate; and  
21 a source region formed in a portion of said substrate proximate said erase gate;  
22 whereby during an erase operation with the drain region, the source region and the  
23 control gate connected to ground, and a relatively high potential applied to the erase gate, stored  
24 electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim  
25 tunneling process.

E1  
Concl'd  
1 9. (Amended) A memory array disposed on a substrate as recited in claim 8 wherein said  
2 floating gate has at least a substantial portion thereof disposed over said channel region and is  
3 separated therefrom by said first insulating layer, said control gate is substantially placed on one  
4 side of said floating gate and separated therefrom by said second insulation layer, said erase gate  
5 is substantially placed on a second side of said floating gate and is separated therefrom by said  
6 second insulation layer, said drain region is substantially disposed on said one side of said  
7 floating gate, and said source region is substantially disposed on said second side of said floating  
8 gate.

1 16. (Amended) A semiconductor device having at least one transistor, the device  
2 comprising:

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3 a substrate having a channel region;  
4 a first insulating layer disposed over said channel region and over at least a portion of  
5 said substrate;

6 a floating gate having at least a substantial portion thereof disposed over disposed over  
7 said channel region and separated therefrom by said first insulating layer, said floating gate  
8 having at least two side walls and a top surface;

9 a second insulating layer disposed over said side walls and over said top surface of said  
10 floating gate;

11 a control gate having a first portion disposed over a first portion of said channel region  
12 and being separated therefrom by said second insulating layer, a second portion formed over a  
13 first one of said side walls and a third portion formed over at least a portion of said top surface of  
14 said floating gate and being separated from said floating gate by said second insulation layer,  
15 said second portion having a surface substantially parallel to and opposing said first one of said  
16 side walls;

17 an erase gate formed over a second one of said side walls and over at least a second  
18 portion of said top surface of said floating gate and being separated from said second one of said  
19 side walls and said portion of said top surface of said floating gate by said second insulation  
20 layer;

21 a source region formed in a portion of said substrate proximate said erase gate; and  
22 a drain region formed in a portion of said substrate proximate said control gate;

23 whereby during an erase operation with the drain region, the source region and the  
24 control gate connected to ground, and a relatively high potential applied to the erase gate, stored  
25 electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim  
26 tunneling process.